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09/842,435	04/25/2001	Brian William Hughes	10004546-1	7471

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	2

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/842,435	Applicant(s) HUGHES ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '103' & '108' in Figure 1; '200', '305', '306', '309' & '311'. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: '409-414' in line 29 on page 10. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: The Related Applications section on page 1 must be updated to include the US Application Serial Application Number to the copending application.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-10, 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites, "if a number of said counted malfunctioning elements **at least equals** a fault threshold" [Emphasis Added]. It is not clear what the Applicant intends by "at least equals". The Examiner assumes the following was intended: -- if a number of said counted malfunctioning elements ~~at least equals~~is less than or equal to a fault threshold --.

Claim 18 recites similar language as in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamae; Takahiko et al. (US 5848077 A, hereafter referred to as Kamae).

35 U.S.C. 102(b) rejection of claim 1.

Kamae teaches a method of evaluating a reliability of a memory segment (Claim 1 and Figures 1 and 8 in Kamae teach a method of evaluating a reliability of an nxm memory cell array segment in an NxM memory array comprising N·M nxm memory cell array segments using Decoder 40 in Figure 8), the method comprising the steps of: counting malfunctioning elements in at least one instance of a defined geometric pattern of said memory segment (col. 5, lines 22-42 in Kamae teach that data is provided with the product error correction code of Figure 7 and each product error correction code word comprising n' rows and m' columns is stored in a single row of a single nxm memory cell array segment, hence each product error correction coded row is a defined geometric pattern of said single nxm memory cell array segment; col. 5, lines 59-63 in Kamae teach that error generation rates during error correction by the first check code are examined to determine if the number of errors generated by cellblock 32, i.e., an n'xm' product error correction code word, exceeds a predetermined number, hence examining error generation is a means for counting errors in the defined geometric pattern of a product error correction coded row to determine which nxm memory cell array segments are malfunctioning); declaring a fault condition within said memory segment if a number of said counted malfunctioning elements at least equals a fault threshold (col. 3, lines 29-31 in Kamae teach an embodiment whereby if more than 100 defective cells are found in an nxm memory cell array segment the nxm memory cell array segment is designated as defective, i.e., malfunctioning); and re-mapping said memory segment in response to said declared fault condition (Figure 6 in Kamae teach that malfunctioning

nxm memory cell array segment (1,3) is mapped to good nxm memory cell array segment (1,4) in response to said declared fault condition).

35 U.S.C. 102(b) rejection of claims 2 and 3.

Malfunctioning elements are counted for a whole nxm memory cell array segment hence are counted in at least one column of said memory segment (col. 3, lines 29-31 in Kamae teach an embodiment whereby if more than 100 defective cells are found in an nxm memory cell array segment the nxm memory cell array segment is designated as defective, i.e., malfunctioning).

35 U.S.C. 102(b) rejection of claim 4.

Malfunctioning elements are counted for a whole nxm memory cell array segment hence are counted in at least one row of said memory segment (col. 3, lines 29-31 in Kamae teach an embodiment whereby if more than 100 defective cells are found in an nxm memory cell array segment the nxm memory cell array segment is designated as defective, i.e., malfunctioning).

35 U.S.C. 102(b) rejection of claim 5.

The Abstract in Kamae teaches a status memory flag for flagging a failed nxm memory cell array segment.

35 U.S.C. 102(b) rejection of claims 6 and 7.

The Abstract in Kamae teaches that only a status memory flag for flagging a failed nxm memory cell array segment is retained hence the count is discarded once the status memory flag is set.

35 U.S.C. 102(b) rejection of claim 8.

The Examiner asserts that col. 5, lines 58-63 of Kamae teaches that check bits are used to check integrity of data after loaded test data is read out of an nxm memory cell array segment. One of ordinary skill in the art at the time the invention was made would have known that error checking for data d with check-bits c occurs by re-encoding data d to produce re-encoded expected check-bits c' whereby c' is compared to c to determine if an error has occurred (Note: comparing c to c' is equivalent to comparing stored d+c to expected data d+c', hence comparing c to c' is a step for comparing read loaded test data to expected data).

35 U.S.C. 102(b) rejection of claim 9.

Col. 3, lines 29-31 in Kamae teach an embodiment whereby if more than 100 defective cells are found in an nxm memory cell array segment the nxm memory cell array segment is designated as defective, i.e., malfunctioning. Defective cells are a characteristic of an nxm memory cell array segment.

35 U.S.C. 102(b) rejection of claim 10.

Col. 3, lines 29-31 in Kamae teach an embodiment whereby if more than 100 defective cells are found in an nxm memory cell array segment the nxm memory cell array segment is designated as defective, i.e., malfunctioning. Since the process is performed for each nxm memory cell array segment the count must be restarted each time a new nxm memory cell array segment is tested.

6. Claims 11-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Harns; Timothy (US 4460997 A).

35 U.S.C. 102(b) rejection of claim 11.

Harns teaches a system for maintaining an operation of a memory segment (the Abstract and col. 6, lines 28-45 in Harns teach a system for maintaining operation of a memory array segment in a multi-array memory by replacing failed rows and columns), the system comprising: means for evaluating elements of said memory segment in row-fast order (col. 5, lines 32-37 in Harns teach a means for evaluating failures in memory element column by column); means for identifying faulty ones of said evaluated elements (PEB Pin Electronics and Error Detection circuit 14 in Figure 1 of Harns is a means for identifying faulty ones of said evaluated elements); means for generating a count of said identified faulty ones of said evaluated elements found for each column of said memory segment (Total Fails Counter 66 is a means for generating a count of said identified faulty ones of said evaluated elements found for each column of said memory array segment); and means for establishing one of a pass condition and a failure

condition for said memory segment based on a value of said count of said identified faulty ones of said evaluated elements (the Abstract and col. 5, lines 32-37 in Harns teach a means for establishing one of a pass condition and a failure condition for said memory segment based on a value of said count of said identified faulty ones of said evaluated elements by flagging the memory array under test as non-repairable).

35 U.S.C. 102(b) rejection of claim 12.

Col. 5, lines 32-37 in Harns teach a means for evaluating failures in memory element column by column, hence Harns teaches a means for preserving information about said generated count for only one column of said memory segment at a time.

35 U.S.C. 102(b) rejection of claim 13.

Col. 5, lines 32-37 in Harns teach a means for evaluating failures in memory element column by column, hence since the count is done column by column for each column, information about said generated count is preserved for only one column of said memory segment at a time and the count is reinitiated for each new column.

35 U.S.C. 102(b) rejection of claim 14.

The Abstract in Harns teaches that when the number of failures in a column exceeds the number of spare rows a flag is established. The number of spare rows is a threshold.

35 U.S.C. 102(b) rejection of claim 15.

The Abstract and col. 6, lines 28-45 in Harns teach a system for maintaining operation of a memory array segment in a multi-array memory by replacing failed rows and columns. Since the tester must be available to test all of the memory array segments in a multi-array memory of a DUT, all values must be reset for the next memory array segment in the multi-array memory to be tested.

35 U.S.C. 102(b) rejection of claim 16.

Total Fails counter 66 in Figure 2 is a means for generating a count comprises: means for incrementing a failure counter upon detecting one of said faulty ones of said evaluated elements.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harns; Timothy (US 4460997 A) in view of Kamae; Takahiko et al. (US 5848077 A, hereafter referred to as Kamae).

35 U.S.C. 103(a) rejection of claim 17.

Harns substantially teaches the claimed invention described in claims 11-16 (as rejected above).

However Harns does not explicitly teach the specific use of re-mapping said memory array segment upon establishment of said failure condition.

Kamae, in an analogous art, teaches re-mapping said memory array segment upon establishment of said failure condition (Figure 6 in Kamae teach that malfunctioning nxm memory cell array segment (1,3) is mapped to good nxm memory cell array segment (1,4) in response to said declared fault condition).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harns with the teachings of Kamae by including use of re-mapping said memory array segment upon establishment of said failure condition.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of re-mapping said memory array segment upon establishment of said failure condition would have provided the opportunity to avoid errors due to defects in the storage media.

35 U.S.C. 103(a) rejection of claim 18.

Harns teaches a system for maintaining an operation of a memory segment (the Abstract and col. 6, lines 28-45 in Harns teach a system for maintaining operation of a memory array segment in a multi-array memory by replacing failed rows and columns), the system comprising: means for evaluating elements of said memory segment in row-fast order (col. 5, lines 32-37 in Harns teach a means for evaluating failures in memory element column by column); means for identifying faulty ones of said evaluated elements (PEB Pin Electronics and Error Detection circuit 14 in Figure 1 of Harns is a means for identifying faulty ones of said evaluated elements); means for generating a count of said identified faulty ones of said evaluated elements found for each column of said memory segment (Total Fails Counter 66 is a means for generating a count of said identified faulty ones of said evaluated elements found for each column of said memory array segment); and means for establishing one of a pass condition and a failure condition for said memory segment based on a value of said count of said identified faulty ones of said evaluated elements (the Abstract and col. 5, lines 32-37 in Harns teach a means for establishing one of a pass condition and a failure condition for said memory segment based on a value of said count of said identified faulty ones of said evaluated elements by flagging the memory array under test as non-repairable).
The Abstract in Harns teaches that when the number of failures in a column exceeds the number of spare rows a flag is established. The number of spare rows is a threshold.

However Harns does not explicitly teach the specific use of re-mapping said memory array segment upon establishment of said failure condition.

Kamae, in an analogous art, teaches re-mapping said memory array segment upon establishment of said failure condition (Figure 6 in Kamae teach that malfunctioning nxm memory cell array segment (1,3) is mapped to good nxm memory cell array segment (1,4) in response to said declared fault condition).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harns with the teachings of Kamae by including use of re-mapping said memory array segment upon establishment of said failure condition. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of re-mapping said memory array segment upon establishment of said failure condition would have provided the opportunity to avoid errors due to defects in the storage media.

35 U.S.C. 103(a) rejection of claim 19.

The Examiner asserts that col. 5, lines 58-63 of Kamae teaches that check bits are used to check integrity of data after stored evaluation data is read out of an nxm memory cell array segment. One of ordinary skill in the art at the time the invention was made would have known that error checking for data d with check-bits c occurs by re-encoding data d to produce re-encoded expected check-bits c' whereby c' is compared to c to determine if an error has occurred (Note: comparing c to c' is equivalent to comparing

stored d+c to expected data d+c', hence comparing c to c' is a step for comparing read stored evaluation data to expected data).

35 U.S.C. 103(a) rejection of claim 20.

Total Fails counter 66 in Figure 2 is a means for generating a count comprises: means for incrementing a failure counter upon detecting one of said faulty ones of said evaluated elements.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eaton; Steven G. et al. (US 4939694 A) teaches a self-testing and self-repairing memory. Hughes; Brian William et al. (US 6373758 B1) teaches a programmable column fail counter for redundancy allocation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133